May 2014

SEPIC Converter Design and Operation

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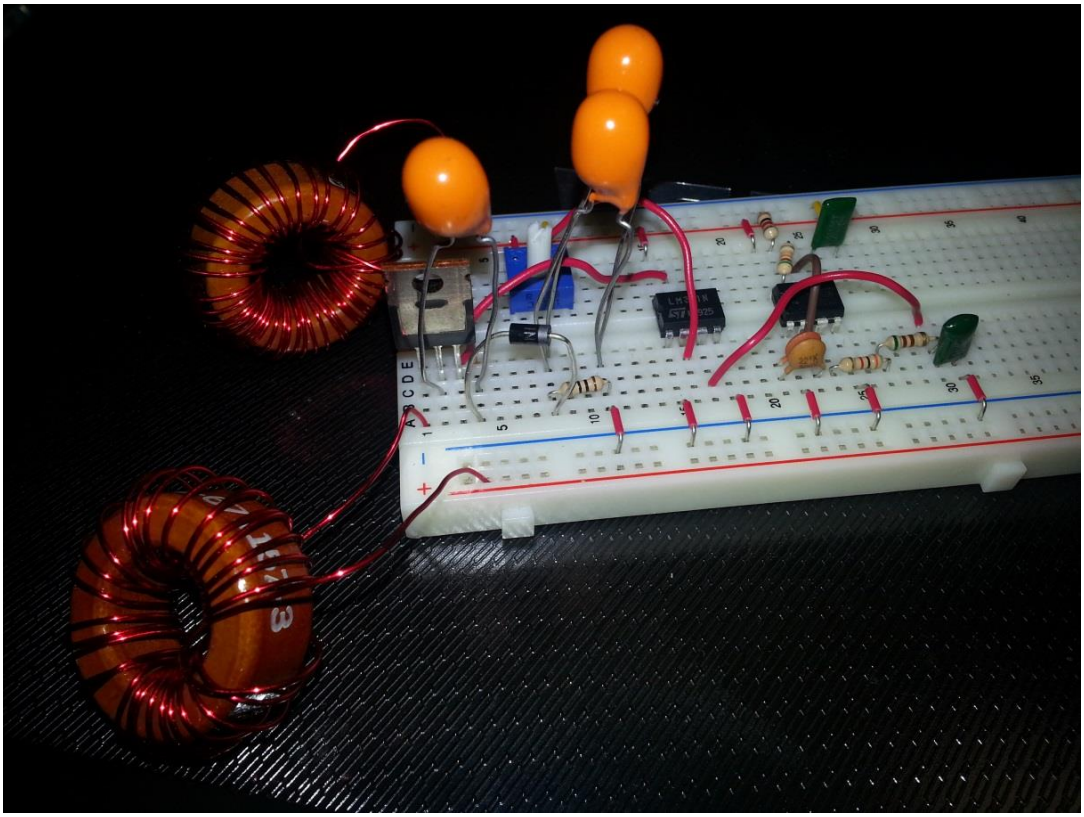
Sepic Converter Design and Operation



Submitted 5/1/14 in partial completion of the requirements for a BS degree from WPI

By

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Table of contents

Table of Figures

I) Abstract

The purpose of this project was to design and optimize a SEPIC dc/dc converter (Single Ended Primary Inductance Converter). The SEPIC converter allows a range of dc voltage to be adjusted to maintain a constant voltage output. This project talks about the importance of dc-dc converters and why SEPIC converters are used instead of other dc-dc converters. This project also goes into detail about how to control the output of the converter with either a potentiometer or feedback to show how it can be implemented in a circuit. From this project, one learns dc-dc converter optimization and control.

II) Introduction

Circuits run best with a steady and specific input. Controlling the input to specific sub-circuits is crucial for fulfilling design requirements. AC-AC conversion can be easily done with a transformer; however dc-dc conversion is not as simple. Diodes and voltage bridges are useful for reducing voltage by a set amount, but can be inefficient. Voltage regulators can be used to provide a reference voltage. Additionally, battery voltage decreases as batteries discharge which can cause many problems if there is no voltage control. The most efficient method of regulating voltage through a circuit is with a dc-dc converter. There are 5 main types of dc-dc converters. Buck converters can only reduce voltage, boost converters can only increase voltage, and buck-boost, Cúk, and SEPIC converters can increase or decrease the voltage.

Some applications of converters only need to buck or boost the voltage and can simply use the corresponding converters. However, sometimes the desired output voltage will be in the range of input voltage. When this is the case, it is usually best to use a converter that can decrease or increase the voltage. Buck-boost converters can be cheaper because they only require a single inductor and a capacitor. However, these converters suffer from a high amount of input current ripple. This ripple can create harmonics; in many applications these harmonics necessitate using a large capacitor or an LC filter. This often makes the buck-boost expensive or inefficient [2]. Another issue that can complicate the usage of buck-boost converters is the fact that they invert the voltage. Cúk converters solve both of these problems by using an extra capacitor and inductor. However, both Cúk and buck-boost converter operation cause large amounts of electrical stress on the components, this can result in device failure or overheating. SEPIC converters solve both of these problems [2].

III) Topology

a) Operation:

All dc-dc converters operate by rapidly turning on and off a MOSFET, generally with a high frequency pulse. What the converter does as a result of this is what makes the SEPIC converter superior. For the SEPIC, when the pulse is high/the MOSFET is on, inductor 1 is charged by the input voltage and inductor 2 is charged by capacitor 1. The diode is off and the output is maintained by capacitor 2. When the pulse is low/the MOSFET is off, the inductors output through the diode to the load and the capacitors are charged. The greater the percentage of time (duty cycle) the pulse is low, the greater the output will be. This is because the longer the inductors charge, the greater their voltage will be. However, if the pulse lasts too long, the capacitors will not be able to charge and the converter will fail as shown in **Fig 3.6**.

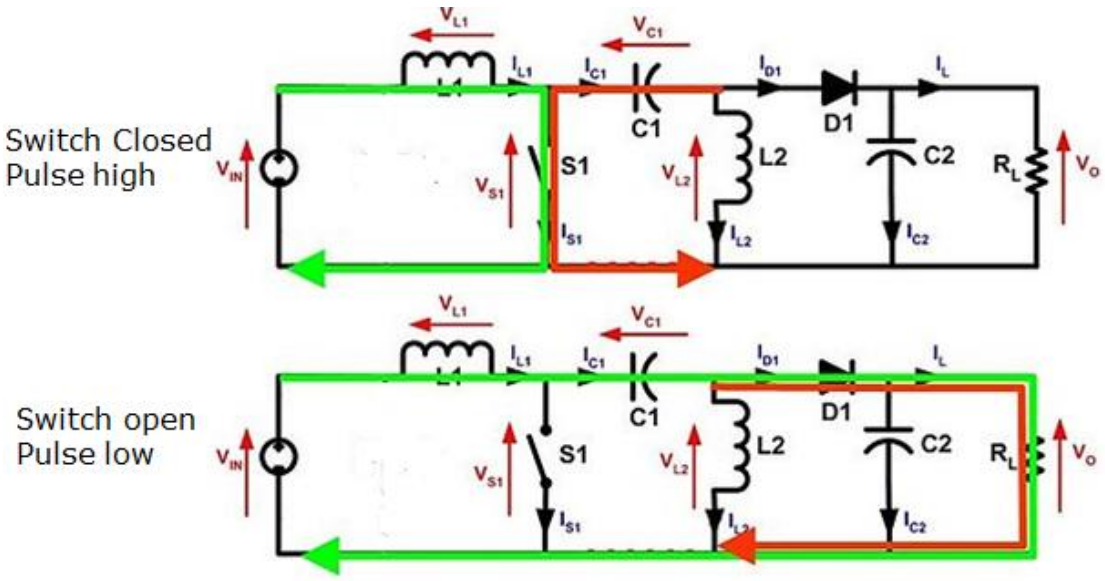

Fig 3.1 SEPIC operation [4]

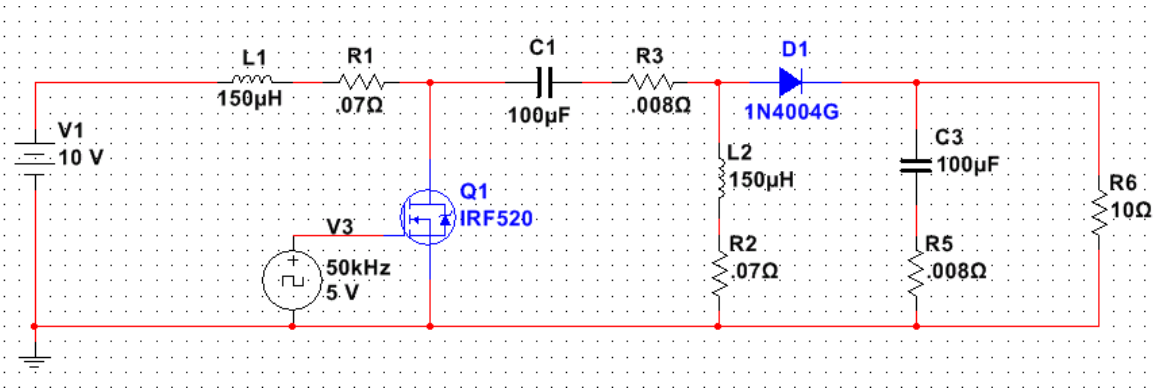

Fig 3.2 SEPIC Simulation

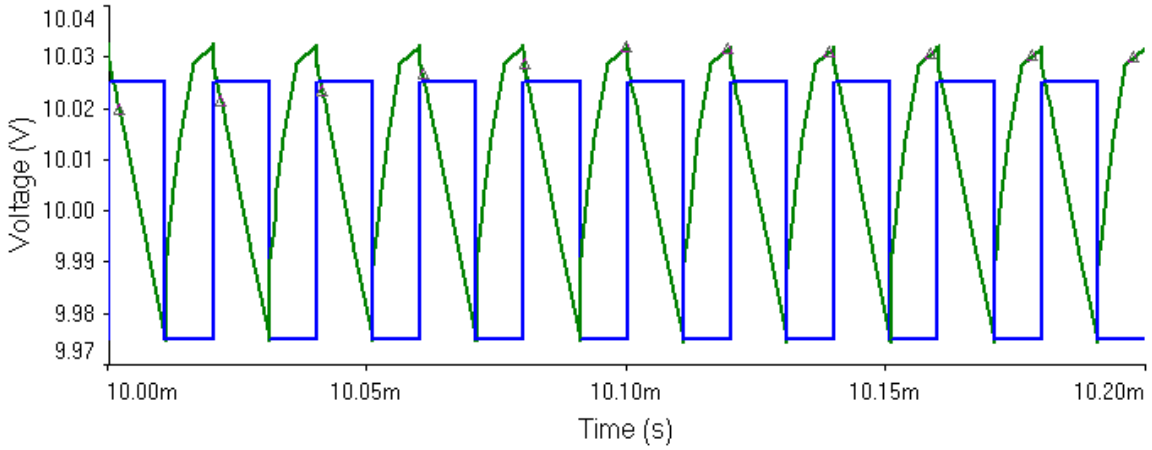

Fig 3.3 Graph of Vout and Pulse

This graph shows the output ripple as a function of the input square wave.

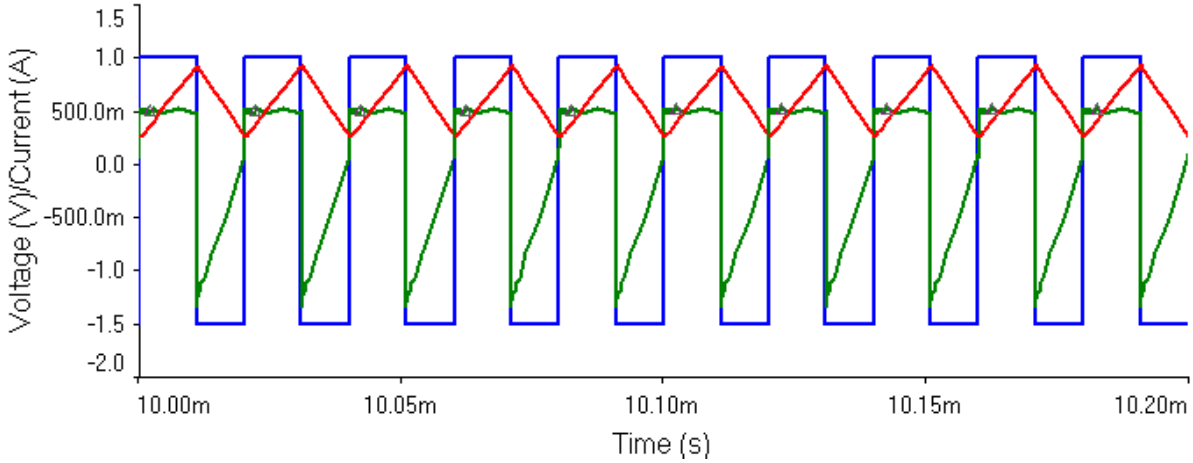

Fig 3.4 Graph of ICout, IL1 and Pulse

This graph shows the ripple in the inductors and how the output capacitor charges and discharges based on the pulse.

b) Specifications:

The converter should meet certain standards

6V<Vin<18V
Vout=10V
Iout=1A
Fsw=50 kHz
An acceptable output current ripple is $\Delta i_{o,\,pp} < 0.5$ A
An acceptable output voltage ripple is $\Delta V_{o,\,pp} < 0.1$ V

c) Duty Cycle Calculation:

The amount that the SEPIC converters step up or down the voltage depends primarily on the

Duty Cycle and the parasitic elements in the circuit.

The output of an ideal SEPIC converter is

$$V_o = \frac{D * V_i}{1 - D}$$

However, this does not account for losses due to parasitic elements such as the diode drop V_D.

These make the equation:

$$V_o + V_D = \frac{D * V_i}{1 - D}$$

This becomes

$$D = \frac{V_o + V_D}{V_i + V_o + V_D}$$

The maximum Duty Cycle will occur when the input voltage is at the minimum. If V_D=.5V, the

Duty Cycle is

$$D_{\min} = \frac{10V + .5V}{6V + 10V + .5V} \approx .64$$

The minimum Duty cycle will occur when the input voltage is at the maximum.

$$D_{\min} = \frac{10V + .5V}{18V + 10V + .5V} \approx .37$$

d) Inductor Calculation:

In theory, the larger the inductors are the better the circuit will operate and reduce the ripple. However, larger inductors are more expensive and have a larger internal resistance. This greater internal resistance will make the converter less efficient. Creating the best converter requires choosing inductors that are just large enough to keep the voltage and current ripple at an acceptable amount.

$$L = \frac{V_{i\min}(D_{\max})}{\Delta i_{o\max} f_{sw}} = \frac{(6V)(.63)}{(.5A)(50kHz)} = 151.2uH$$

Inductors with low internal resistance and around 150uH will be ideal for both of the inductors in the circuit.

e) Simulation Results:

SEPIC WITH PARASITICS

```
V       1       0       10
RL1     1       1.5     .07
L1      1.5     2       150u    IC=0
S       2       0       20      0       SWK
.MODEL      SWK     VSWITCH (RON=.2  ROFF=1MEG VON=1          VOFF=0)
VP      20      0       PULSE (0        10      0       1n      1n      .01045m         .02m)
RCl     2       2.5     .08
C1      2.5     3       10u     IC=0
L2      3       3.5     150u    IC=0
RL2     3.5     0       .07
D       3       4       Dix
.MODEL      Dix     D (RS= .07      BV=480          N=.01)
C2      4       4.5     100u    IC=0
RC2     4.5     0       .08
R       4       0       10
.PROBE
.TRAN           .005    .1      .099    10u     UIC
.END
```

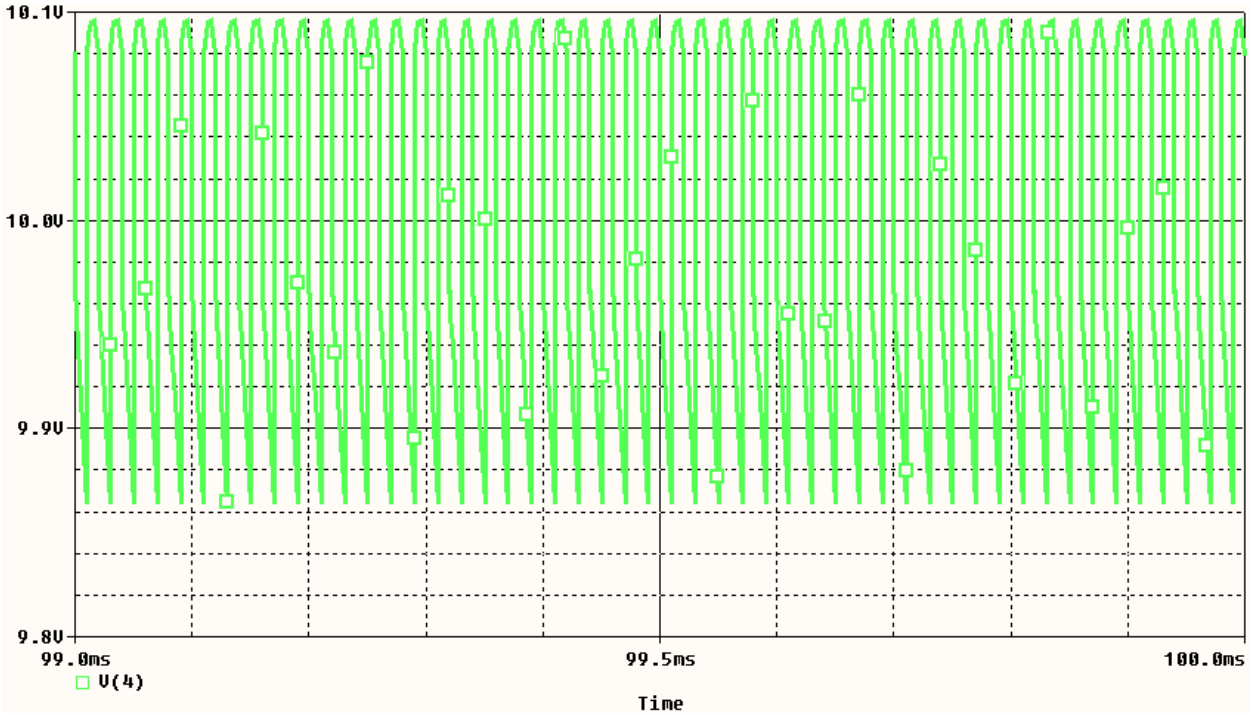

Fig 3.5 Graph of Vout

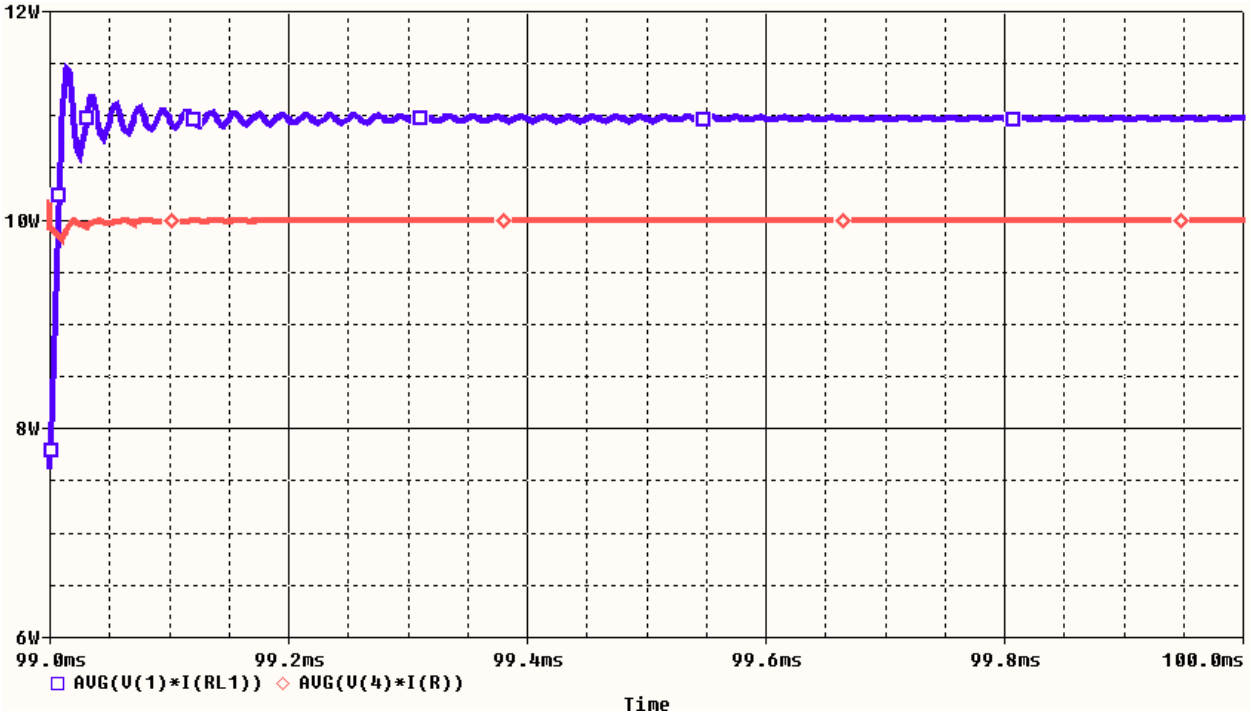

Fig 3.6 Graph of Pout and Pin

This graph shows that the efficiency of the Converter=Pin/Pout= .91

SEPIC AVERAGED MODEL WITH PARASITICS AND D INCREASING FROM 0 TO 1

```
VC      30      0       PWL (0, 0 100m, 1)                          D increasing from 0 to 1
V       1       0       10
L1      1       1.5     150u IC=0
RL1     1       2       .3
VD      2       3       0
E       3       20      Value= {(1-V(30))/V(30)*V(5)}               MOSFET V=Vo*(1-D)/D
VF      20      0       0
C1      3       3.5     1u      IC=0
RC1     3.5     4       .08
L2      4       4.5     150u    IC=0
RL2     4.5     0       .3
G       4       5       Value={((1-V(30))/(V(30)*V(30)))*I(VF)}     Diode I =Iin*(1-D)/D^2
C2      5       5.5     100u    IC=0
RC2     5.5     0       .08
R       5       0       10
.PROBE
.TRAN           0       .1      0       10u     UIC
.END
```

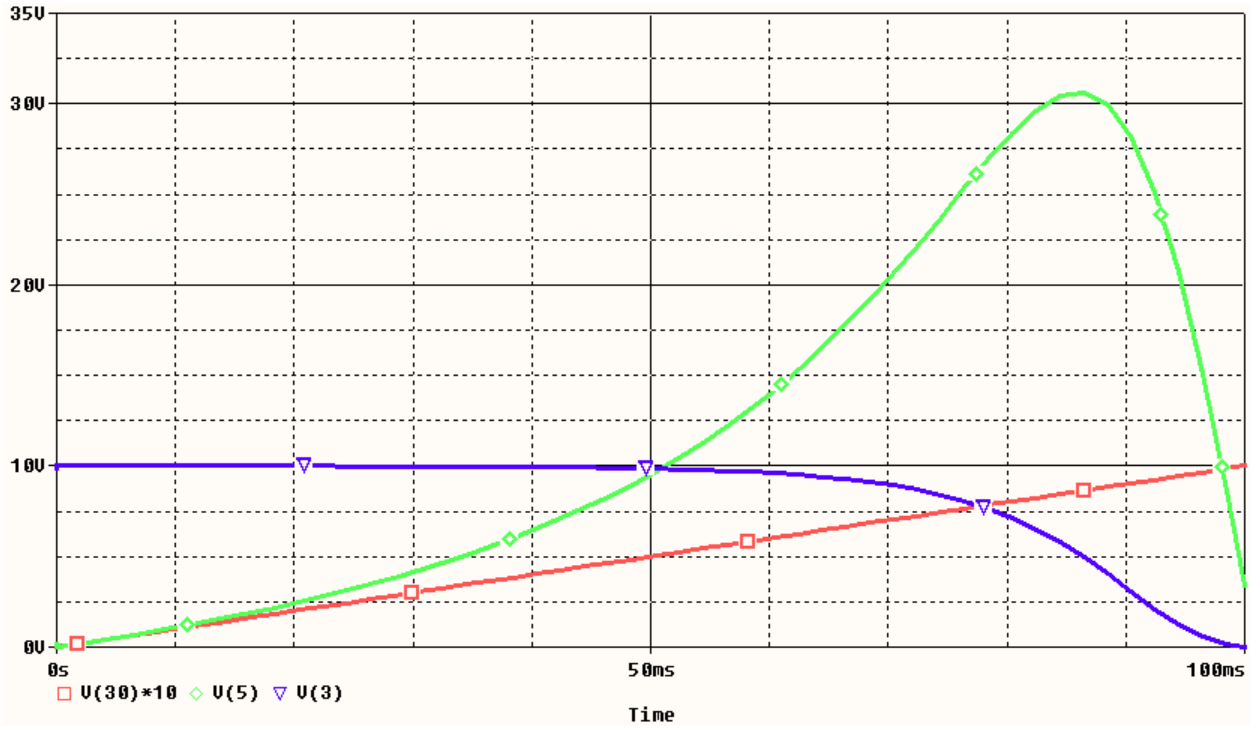

Fig 3.7 Graph of Vout, D and VCin with Vin=10V

This graph shows that as D increases from 0 to 1, Vout increases exponentially, reaching Vin around D=.5. When D gets too high, VCin cannot stay charged and this causes Vout to drop as well.

IV) Potentiometer Controlled PWM

The SEPIC converter is able to either increase or decrease an input voltage by controlling the Duty Cycle of a pulse to the MOSFET. One way to do that is to directly control the Duty cycle using a potentiometer. There are some applications for which this control method is suitable but it is insufficient for many other applications.

In order to drive the MOSFET, a pulse is needed. A 555 timer is used to produce a square wave with a set frequency and a Duty cycle≥50%. However, the duty cycle from the 555 cannot be easily changed without switching resistors. In addition, the SEPIC requires a duty cycle below 50% to buck the voltage when the input voltage is low. The pulse width will need to be modified separately from the 555 because the 555 cannot change or produce a duty cycle less than 50%. First a resistor and a capacitor are used in lowpass to produce a triangle wave from the square wave output of the 555. Afterwards, this is sent to the negative pin of a comparator. The positive pin of the comparator receives a controlled voltage signal. Whenever the controlled voltage is greater than the triangle wave, the comparator will output voltage and otherwise it will be off. The greater this signal, the greater the duty cycle of the comparator output will be. One way to control this signal is to step down voltage using a potentiometer. Luckily, this signal can be kept in the same range as the triangle wave by using the same input that drives the 555 timer. The duty cycle will not change when the input or the output voltage changes which means there is full control of how much the SEPIC steps up or down the voltage. This has both advantages and disadvantages for the circuit.

Full control of the circuit can be useful. The potentiometer allows the SEPIC to output a wide range of voltage from a wide range of input. This could be useful in battery applications

that need to run on various levels of power. One example would be a flashlight with adjustable brightness. This SEPIC converter could allow it to run on a large range of power with greater efficiency than simply reducing the voltage with a potentiometer to control the output. However, this control method does have its drawbacks.

Most applications of the SEPIC converter control the voltage automatically. The problem with relying on controlling the input for circuit control is that there is no circuit feedback. When using a potentiometer, the only way to maintain the correct output is to watch the output and adjust accordingly. Visual feedback is only useful in certain circumstances. Usually it is best to use the SEPIC converter to hold a single output without the need for control when using a SEPIC as part of a large circuit.

a) PWM Demonstration

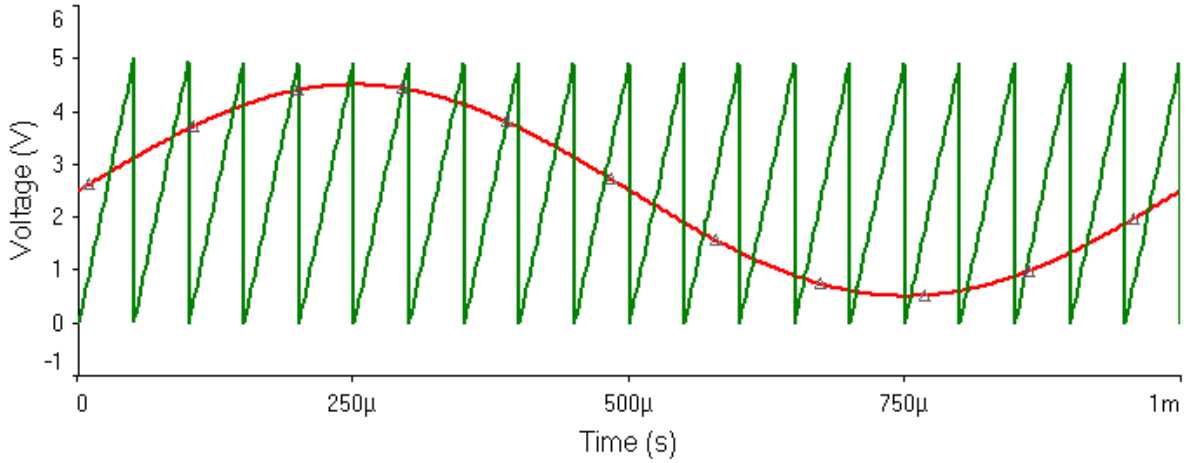

Fig 4.1 Graph of Triangle wave and Sinusoidal control wave

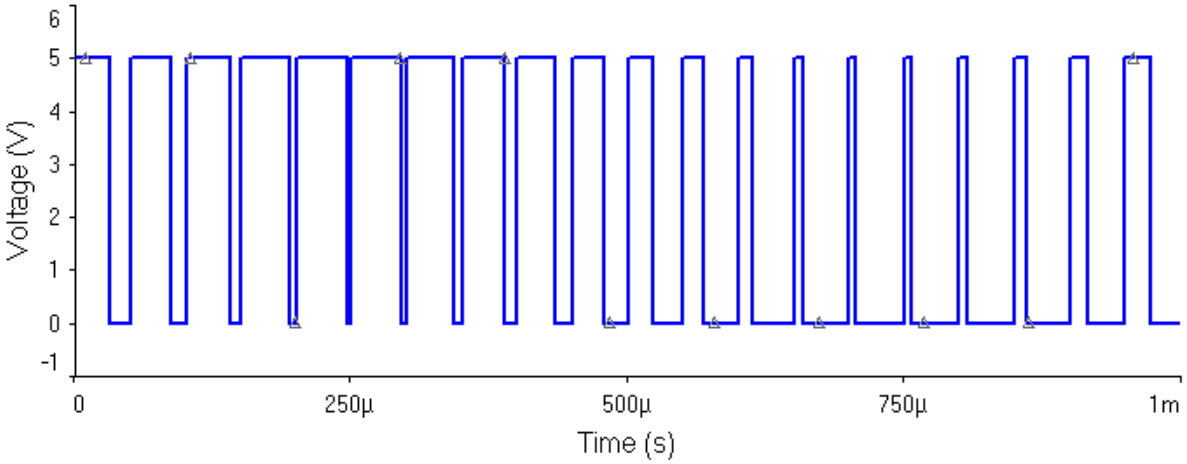

Fig 4.2 Graph of controlled square wave

This graph shows the resulting output of the comparator with the inputs shown in **Fig 4.1**. The pulse is high when the control signal is greater than the triangle wave. This results in a higher duty for high control signals.

b) Circuit Diagram

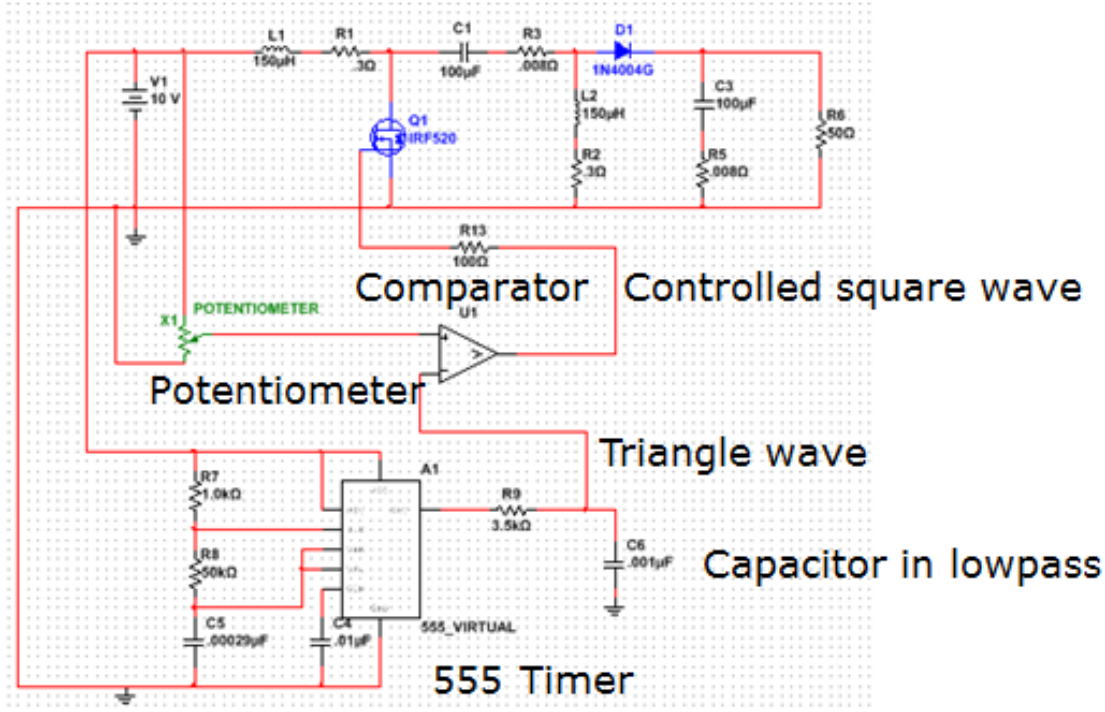

Fig 4.3 Labelled schematic of SEPIC converter using a potentiometer to control PWM.

c) Simulation Results

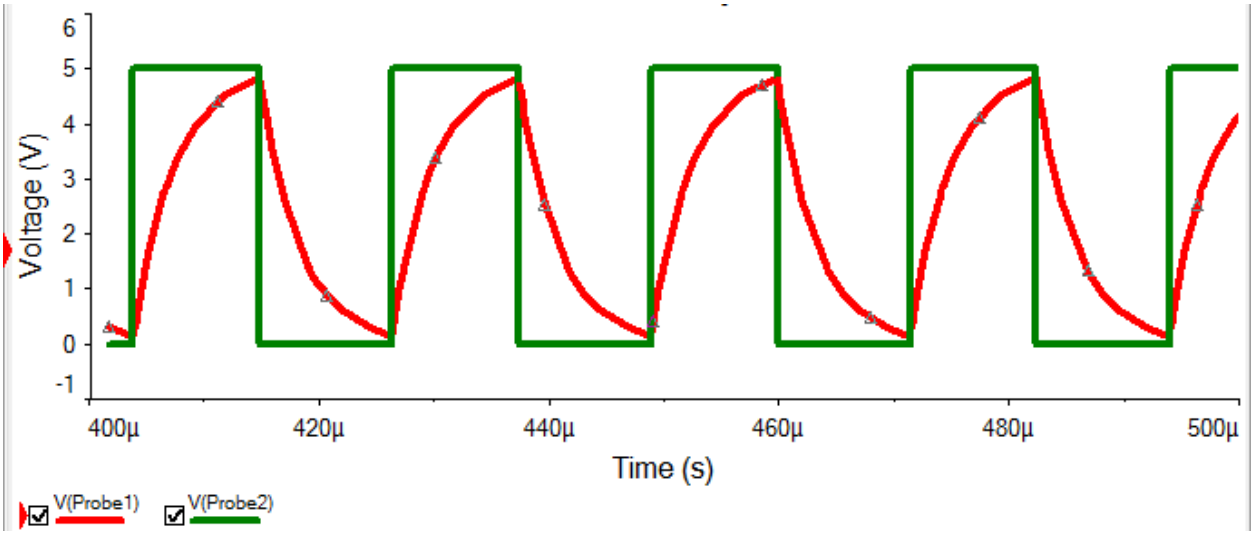

Fig 4.4 Graph of 555 and Triangle wave

This is the output of the 555 with the triangle wave produced by the capacitor in lowpass.

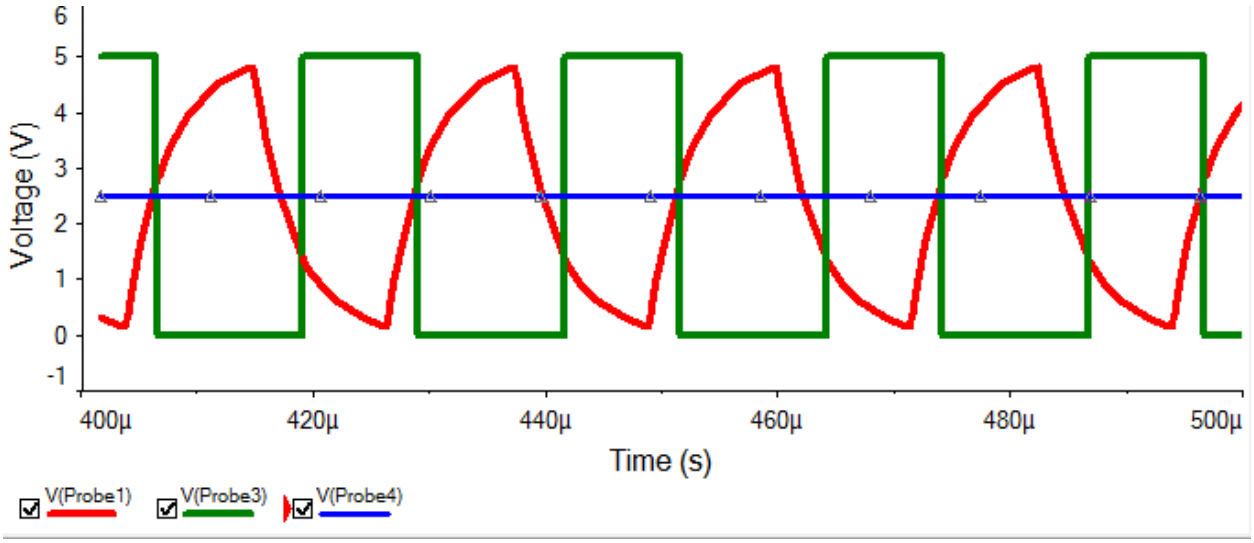

Fig 4.5 Graph of Comparator output to MOSFET, Triangle Wave and Control Signal from Potentiometer

This graph shows that the comparator turns on soon after the triangle wave falls below the control signal (which is a simulation error) and turns off immediately when the triangle wave rises above the signal.

V) Feedback Controlled PWM

While a potentiometer allows for control of the SEPIC converter output during operation, it is unable to hold a constant output with a variable input that changes. This is used in the majority of SEPIC converter applications which require automation to correct an input voltage. The simplest way to maintain a constant output is to use a feedback loop that will change the output automatically instead of by manual control (using visual feedback from a voltmeter). The feedback loop should be able to increase the duty cycle to raise the output when the output is too low and decrease it when the output is too high. To do this, the output will need to be compared to a reference voltage which remains constant even if the input changes. The error between the output and the reference voltage is then amplified and added to a set bias voltage. The resulting voltage is then used as the control voltage for PWM. When the output is too low, the amplified error increases which causes the control voltage to increase. The increase in control voltage increases the duty cycle until the output is correct. When the output is too high, the amplified error becomes negative which decreases the duty cycle to correct output. Both of these scenarios work together to constantly make slight adjustments to the duty cycle so that the output remains stable. The simulations for feedback show how the output changes with the gain of the amplifier

a) Feedback Flow Chart

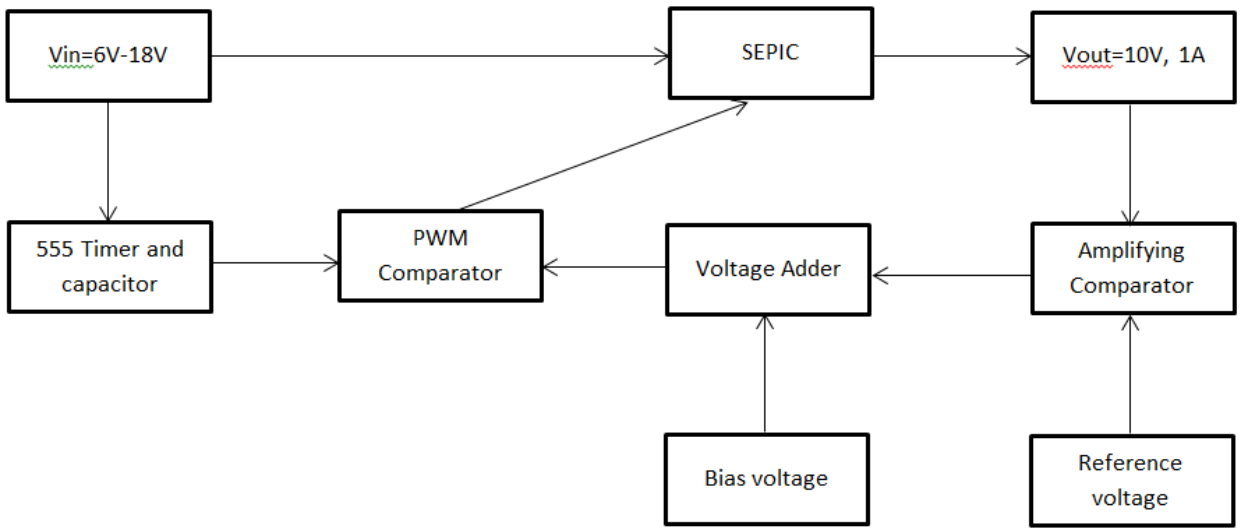

Fig 5.1 Flow chart for feedback operation

b) Feedback Results at Various Levels of Gain

SEPIC AVERAGED MODEL WITH FEEDBACK

Feedback loop

Gain

```
Ve      30      0       10
Ee      33      0       Value={(1+7*(V(30,0)-V(5,0)))}
Eb      34      0       Value={.5*(1+(V(30,0)+V(33,0))/10)}
```

Gain*(Vref-Vo)= Gain*Error
this value equals D

SEPIC averaged model

```
V       .5      0       0
VC      1       .5      PWL(0,0 100m, 20)
L1      1       1.5     150u IC=0
RL1     1       2       .07
VD      2       3       0
E       3       20      Value={(V(34,0)-1)/V(34,0)*V(5,0)}
VF      20      0       0
C1      3       3.5     1u      IC=0
RC1     3.5     4       .08
L2      4       4.5     150u    IC=0
RL2     4.5     0       .07
G       4       5       Value={(V(34,0)-1)/(V(34,0)*V(34,0))
C2      5       5.5     100u    IC=0
RC2     5.5     0       .08
R       5       0       10
.PROBE
```

.TRAN 0 .1 0 10m UIC
.END

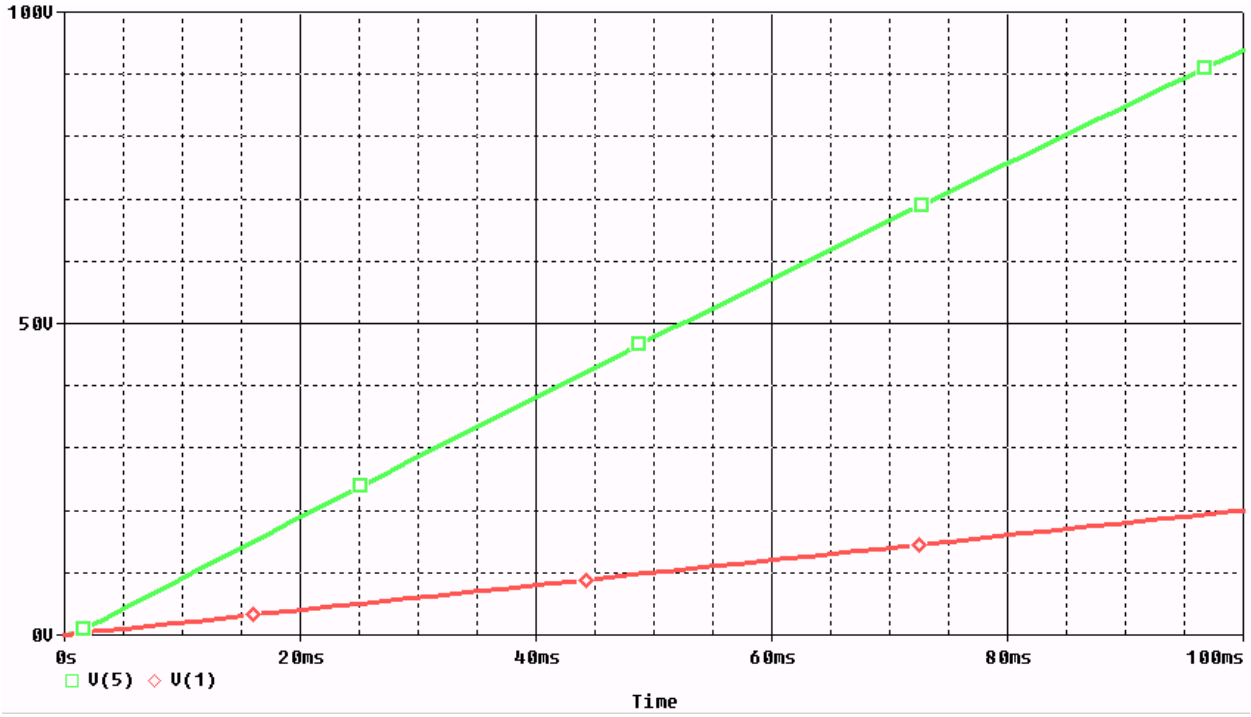

Fig 5.2 Graph of Vout, as Vin increases. Gain is almost zero

This graph shows that if the gain of the amplifier is around zero, Vout is uncontrolled.

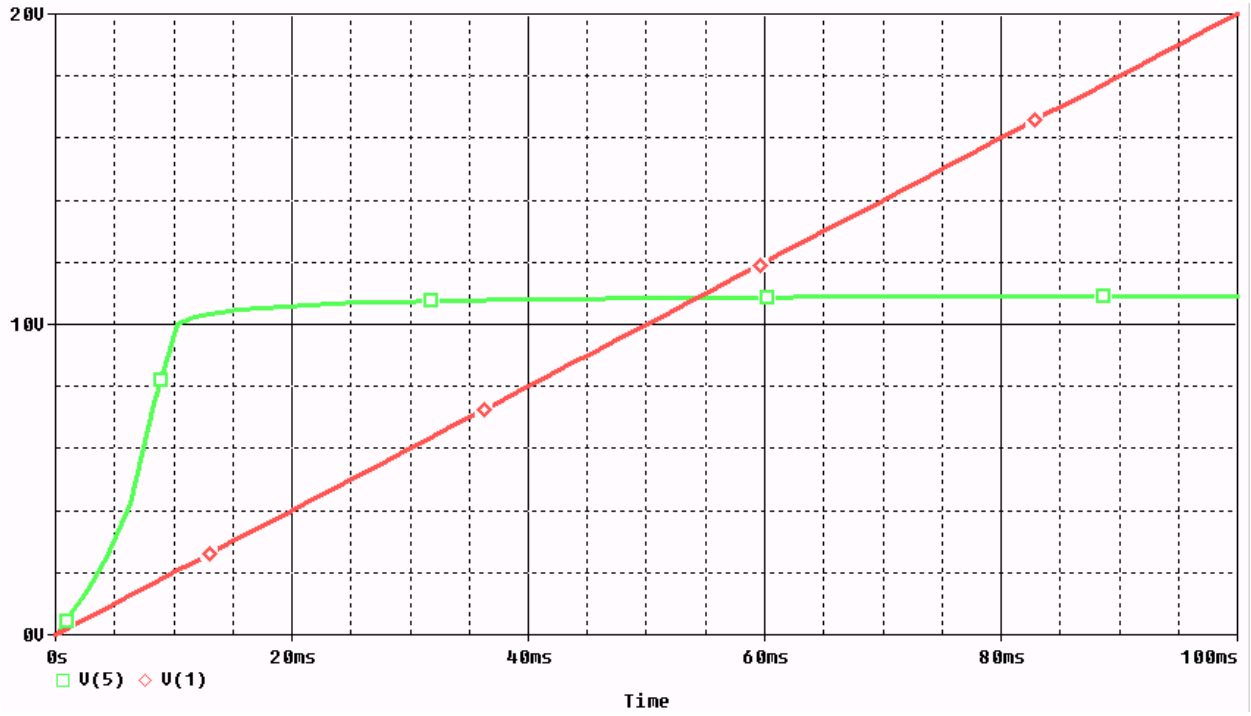

Fig 5.3 Graph of Vout, as Vin increases. Gain is too low

This graph shows that if the gain of the amplifier is too low, Vout is controlled, but too high.

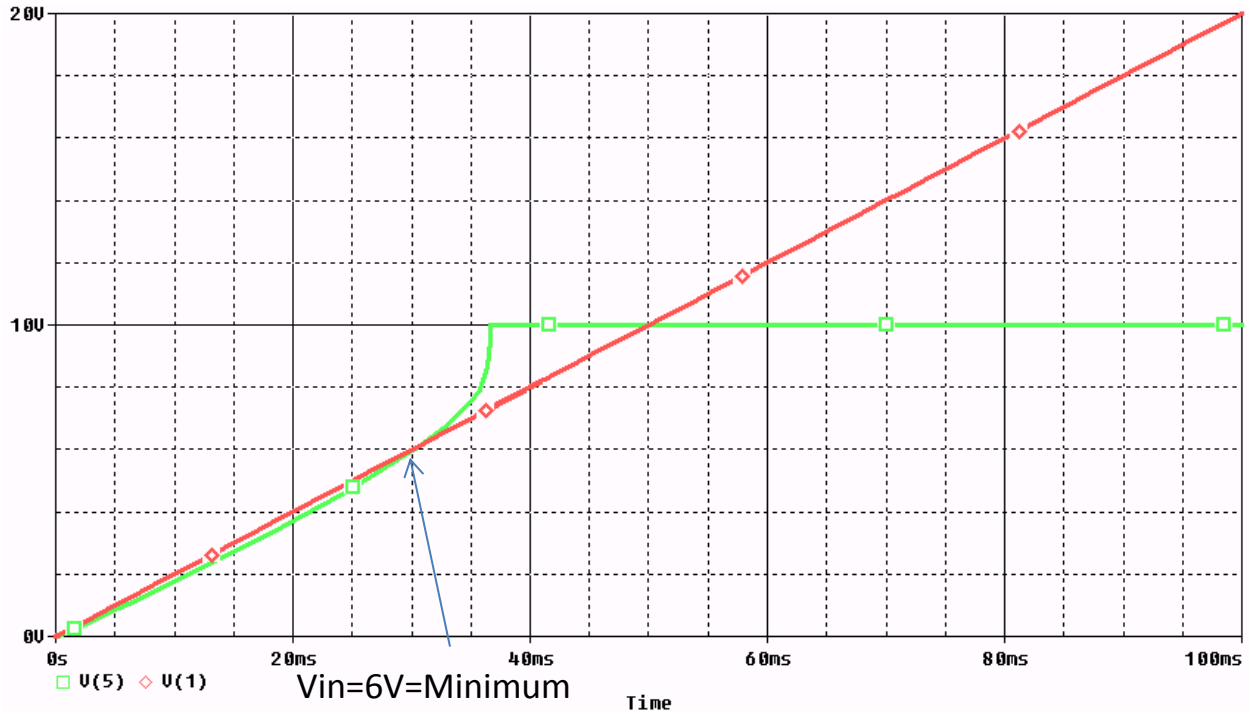

Fig 5.4 Graph of Vout, as Vin increases. Gain is too high

This graph shows that if the gain of the amplifier is too high, the converter cannot boost sufficiently and Vout does not reach 10V until after Vin is greater than the minimum value.

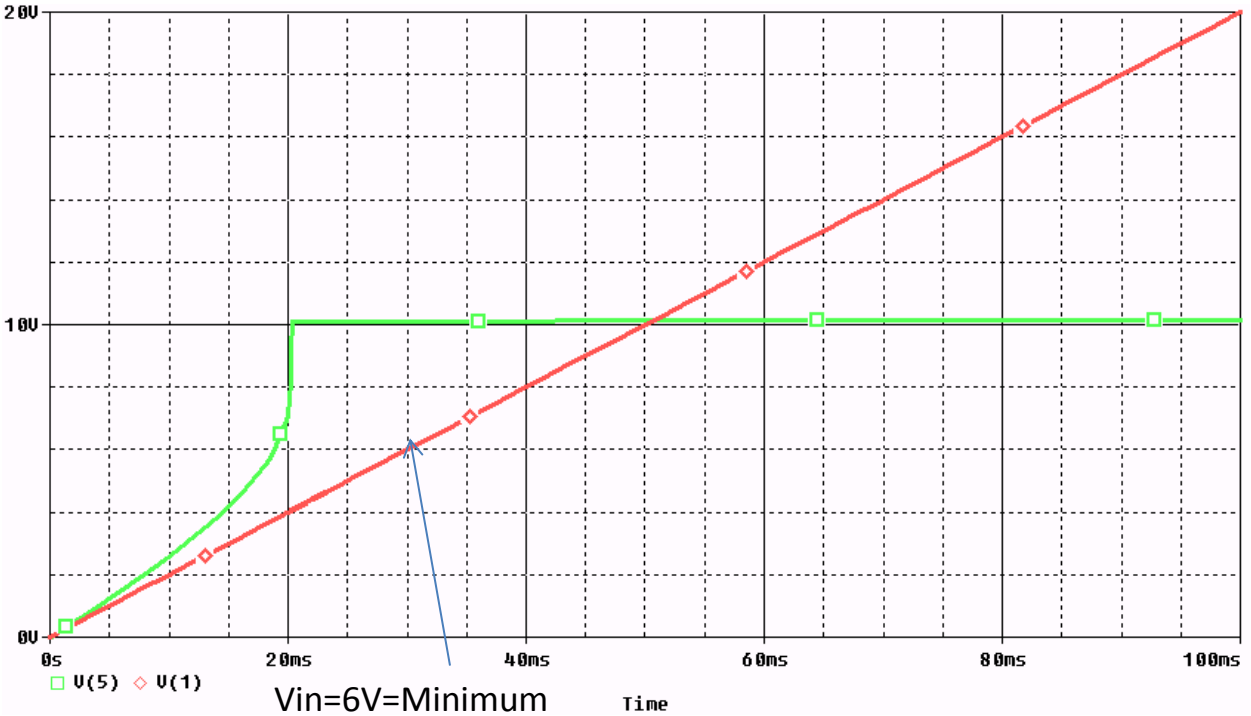

Fig 5.5 Graph of Vout, as Vin increases. Gain is at a good value

This graph shows that with the correct amount of gain, Vout will be at the correct value as long as Vin is greater than the minimum value.

VI) Summary

Most battery operated circuits require dc-dc conversion to maintain full operation. In most circumstances that require stepping up and down the input voltage, SEPIC converters are worth the price of the extra inductor and capacitor for the efficiency and stable operation they provide. While this project does go into detail about simulation results for the SEPIC converter, the physical potentiometer controlled SEPIC converter built was unsuccessful. Additionally, a cost benefit analysis to determine peak efficiency with the cheapest cost for the inductors and capacitors was never done. These are both things that could have been done with extra time and group members. From this project, one learns dc-dc converter optimization and control.

VII) References

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3. Durán, E. Sidrach-de-Cardona, M. Galán, J. Andújar, J.M. “Comparative Analysis of Buck-Boost Converters used to obtain I-V Characteristic Curves of Photovoltaic Modules” April 2014 <http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=04592243>

Pictures from

[4] Wikipedia user Mclausma <http://en.wikipedia.org/wiki/File:S1_open.jpg> <http://en.wikipedia.org/wiki/File:S1_closed.jpg>